THAT WHICH IS CLAIMED IS:

1. A method of fabricating a transistor, comprising:

forming a nitride-based semiconductor barrier layer on a nitride-based semiconductor channel layer;

forming a protective layer on a gate region of the nitride-based semiconductor barrier layer;

forming patterned ohmic contact metal regions on the barrier layer;

annealing the patterned ohmic contact metal to provide first and second ohmic contacts, wherein the annealing is carried out with the protective layer on the gate region; and

forming a gate contact on the gate region of the barrier layer.

2. The method of Claim 1, further comprising removing the protective layer subsequent to annealing the patterned ohmic contact metal.

3. The method of Claim 2, wherein the protective layer comprises an aluminum nitride layer.

4. The method of Claim 2, wherein removing the protective layer comprises removing the protective layer utilizing a low damage etching technique.

5. The method of Claim 4, wherein the low damage etching technique comprises a wet etch using a strong base.

6. The method of Claim 2, wherein removing the protective layer is followed by forming a passivation layer on exposed portions of the barrier layer.

7. The method of Claim 6, wherein forming a gate contact comprises:

etching a recess in the passivation layer utilizing a low damage etch technique to expose a portion of the gate region of the barrier layer; and

forming the gate contact in the recess in the passivation layer.

8. The method of Claim 1, wherein forming a gate contact comprises forming a gate contact on the protective layer on the gate region of the barrier layer.

9. The method of Claim 1, further comprising forming a passivation layer on exposed portions of the barrier layer and the protective layer.

10. The method of Claim 9, wherein forming a gate contact comprises forming a gate contact that extends through the passivation layer and the protective layer to contact the barrier layer.

11. The method of Claim 1, wherein forming a protective layer comprises forming a patterned protective layer on the barrier layer, the patterned protective layer covering a first portion of the barrier layer corresponding to the gate region and exposing adjacent second portions of the barrier layer corresponding to the first and second ohmic contacts; and

wherein forming patterned ohmic contact metal regions comprises forming patterned ohmic contact metal regions on the second portions of the barrier layer, the patterned ohmic contact metal regions being adjacent and spaced apart from the patterned protective layer.

12. The method of Claim 11, wherein forming a patterned protective layer comprises:

blanket depositing a protective layer material on the barrier layer;

forming a mask on the blanket deposited protective layer material, the mask having windows corresponding to locations of the first and second ohmic contacts;

etching the blanket deposited protective layer through the windows utilizing a low damage etching technique; and

removing the mask.

13. The method of Claim 12, wherein the windows corresponding to locations of the first and second ohmic contacts are larger than an area of the first and second ohmic contacts.

14. The method of Claim 12, wherein forming patterned ohmic contact metal regions on the second portions of the barrier layer, the patterned ohmic contact metal regions being adjacent and spaced apart from the patterned protective layer is carried out prior to removing the mask.

15. The method of Claim 11, wherein forming a gate contact comprises:

forming a recess in the patterned protective layer that exposes a portion of the first portion of the barrier layer; and

forming a gate contact in the recess.

16. The method of Claim 15, wherein forming a recess comprises:

forming a mask on the patterned protective layer, the mask having a window corresponding to a location of the recess;

etching the patterned protective layer through the window utilizing a low damage etching technique; and

removing the mask.

17. The method of Claim 16, wherein the low damage etching technique utilized to etch the patterned protective layer comprises a wet etch with a strong base.

18. The method of Claim 15, wherein forming a gate contact in the recess is followed by forming a passivation layer on the patterned protective layer and in a gap between the patterned protective layer and the first and second ohmic contacts.

19. The method of Claim 11, wherein the protective layer comprises SiN.

20. The method of Claim 11, wherein the protective layer comprises AlN.

21. The method of Claim 11, wherein the protective layer comprises SiO_2.

22. The method of Claim 11, further comprising forming a passivation layer on the patterned protective layer and so as to substantially fill gaps between the patterned protective layer and the first and second ohmic contacts.

23. The method of Claim 22, wherein the patterned protective layer and the passivation layer comprise a same material.

24. The method of Claim 22, wherein the patterned protective layer comprises aluminum nitride and the passivation layer comprises silicon nitride.

25. The method of Claim 11, further comprising removing the patterned protective layer so as to expose the first portion of the barrier layer.

26. The method of Claim 25, wherein removing the patterned protective layer is followed by forming a passivation layer on exposed portions of the barrier layer.

27. The method of Claim 26, wherein the patterned protective layer comprises aluminum nitride and the passivation layer comprises silicon nitride.

28. The method of Claim 26, wherein forming a gate contact is preceded by forming a passivation layer and wherein forming a gate contact comprises:

forming a recess in the passivation layer that exposes a portion of the first portion of the barrier layer; and

forming a gate contact in the recess.

29. The method of Claim 28, wherein forming a recess comprises:

forming a mask on the passivation layer, the mask having a window corresponding to location of the recess;

etching the passivation layer through the window utilizing a low damage etching technique; and

removing the mask.

30. The method of Claim 1, further comprising

forming a Group III-nitride layer to provide the nitride-based channel layer; and

wherein forming a nitride-based semiconductor barrier layer comprises forming a Group III-nitride layer.

31. The method of Claim 30, wherein the channel layer has a composition of $Al_xGa_{1-x}N$ wherein $0 \leq x < 1$, and wherein the bandgap of the channel layer is less than the bandgap of the barrier layer.

32. The method of Claim 31:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN); and

wherein the barrier layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN.

33. The method of Claim 1, wherein the barrier layer comprises multiple layers.

34. The method of Claim 1 further comprising:

forming a buffer layer on a substrate; and

forming a Group III-nitride channel layer on the buffer layer to provide the nitride-based channel layer.

35. The method of Claim 1, where the channel layer and the barrier layer are configured to provide a High Electron Mobility Transistor (HEMT).

36. The method of Claim 1, wherein the nitride-based channel layer is provided on a SiC substrate.

37. The method of Claim 11, wherein forming a gate contact is preceded by forming a passivation layer and wherein forming a gate contact comprises:

forming a recess in the passivation layer and the patterned protective layer that exposes a portion of the first portion of the barrier layer; and

forming a gate contact in the recess.

38. The method of Claim 11, wherein the protective layer is formed to a thickness of at least about a thickness of the ohmic contact material and wherein the gate is directly on the protective layer.

39. The method of Claim 1, wherein the protective layer has a thickness of at least about two monolayers.

40. The method of Claim 1, wherein the protective layer has a thickness of from about 5 nm to about 500 nm.

41. A high electron mobility transistor comprising:

a nitride-based channel layer on a substrate;

a nitride-based semiconductor barrier layer on the nitride-based channel layer, the nitride based semiconductor barrier layer having a sheet resistance that is substantially the same as an as-grown sheet resistance of the nitride-based semiconductor barrier layer;

ohmic contacts on the barrier layer; and

a gate contact on the barrier layer.

42. The high electron mobility transistor of Claim 41, further comprising a protective layer disposed on the barrier layer that is adjacent and spaced apart from the ohmic contacts and that the gate contact extends through.

43. The high electron mobility transistor of Claim 42, further comprising a passivation layer on the protective layer and that substantially fills a gap between the ohmic contacts and the protective layer.

44. The high electron mobility transistor of Claim 43, wherein the passivation layer is also on the protective layer and wherein the gate contact extends through the protective layer and the passivation layer.

45. The high electron mobility transistor of Claim 43, wherein at least a portion of the gate contact is directly on the protective layer and a portion of the gate contact is directly on the barrier layer.

46. The high electron mobility transistor of Claim 41, further comprising a passivation layer on the barrier layer that substantially fills a gap between the ohmic contacts and the gate contact.

47. The high electron mobility transistor of Claim 41:

wherein the nitride-based channel layer comprises a Group III-nitride layer; and

wherein the nitride-based semiconductor barrier layer comprises a Group III-nitride layer.

48. The high electron mobility transistor of Claim 41, wherein the channel layer has a lower bandgap than the barrier layer.

49. The high electron mobility transistor of Claim 41, wherein the channel layer comprises an undoped layer having a thickness of greater than about 20 Å.

50. The high electron mobility transistor of Claim 41, wherein the channel layer comprises a superlattice and/or a combination of Group III-nitride layers.

51. The high electron mobility transistor of Claim 41:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN); and

wherein the barrier layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN.

52. The high electron mobility transistor of Claim 41, wherein the barrier layer comprises $Al_xGa_{1-x}N$ wherein $0 < x < 1$.

53. The high electron mobility transistor of Claim 41, wherein the barrier layer comprises multiple layers.

54. The high electron mobility transistor of Claim 41, further comprising a buffer layer on the substrate, and wherein the nitride-based channel layer is disposed on the buffer layer.

55. The high electron mobility transistor of Claim 42, wherein the protective layer has a thickness of at least as thick as the ohmic contacts.

56. The high electron mobility transistor of Claim 41, wherein the ohmic contacts have a contact resistance of less than about 1 Ω-mm.

57. A high electron mobility transistor, comprising:

a nitride-based channel layer on a substrate;

a nitride-based semiconductor barrier layer on the nitride-based channel layer;

a protective layer on the barrier layer;

ohmic contacts on the barrier layer, adjacent and spaced apart from the protective layer so as to provide a gap between the ohmic contacts and the protective layer; and

a gate contact on the barrier layer and extending through the protective layer.

58. The high electron mobility transistor of Claim 57, further comprising a passivation layer on the protective layer and that substantially fills the gap between the ohmic contacts and the protective layer.

59. The high electron mobility transistor of Claim 57:

wherein the nitride-based channel layer comprises a Group III-nitride layer; and

wherein the nitride-based semiconductor barrier layer comprises a Group III-nitride layer.

60. The high electron mobility transistor of Claim 57, wherein the channel layer has a lower bandgap than the barrier layer.

61. The high electron mobility transistor of Claim 57, wherein the channel layer comprises an undoped layer having a thickness of greater than about 20 Å.

62. The high electron mobility transistor of Claim 57, wherein the channel layer comprises a superlattice and/or a combination of Group III-nitride layers.

63. The high electron mobility transistor of Claim 57:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN); and

wherein the barrier layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN.

64. The high electron mobility transistor of Claim 57, wherein the barrier layer comprises $Al_xGa_{1-x}N$ wherein $0 < x < 1$.

65. The high electron mobility transistor of Claim 57, wherein the barrier layer comprises multiple layers.

66. The high electron mobility transistor of Claim 57, further comprising a buffer layer on the substrate, and wherein the nitride-based channel layer is disposed on the buffer layer.

67. The high electron mobility transistor of Claim 57, wherein the protective layer is at least as thick as the ohmic contacts.

68. The high electron mobility transistor of Claim 67, wherein the gate contact is directly on the protective layer.

69. The high electron mobility transistor of Claim 57, wherein the protective layer has at thickness of about two monolayers.

70. A method of fabricating a transistor, comprising:

forming a nitride-based semiconductor barrier layer on a nitride-based semiconductor channel layer;

forming a protective layer on a gate region of the nitride-based semiconductor barrier layer;

forming patterned ohmic contact metal regions on the barrier layer;

annealing the patterned ohmic contact metal to provide first and second ohmic contacts;

etching a recess in the protective layer in a gate region of the barrier layer utilizing a low damage etch technique to expose a portion of the gate region of the barrier layer; and

forming the gate contact in the recess in the passivation layer.

71. The method of Claim 70, wherein the protective layer comprises a passivation layer.

72. The method of Claim 70, wherein the protective layer comprises an aluminum nitride layer, a silicon nitride layer and/or a silicon dioxide layer.

73. The method of Claim 70, wherein the low damage etching technique comprises a wet etch using a strong base.

74. The method of Claim 70, wherein annealing the patterned ohmic contact metal to provide first and second ohmic contacts is carried out prior to forming a protective layer.

75. The method of Claim 70, wherein annealing the patterned ohmic contact metal to provide first and second ohmic contacts is carried out subsequent to forming a protective layer.